EAST - [09323986.wsp:1]

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Drafts
Pending
Active
L1: (25811) dram
L2: (67613) polysilicon
L3: (338) cell and 1 and 2
L4: (6915) spin adj3 glass
L5: (9728) 4 sog
L6: (6915) 3 and 4
L7: (193) 5 and 3
L8: (4662) 6 and oxide
L9: (95) 7 and [illegible]
Failed
Saved
(96375) (bendable flexible moveable) with (frame container supporter)
(1805) ((chip die dice ic (integrated adj circuit)) same (bendable flexible moveab
(1283) (bendable flexible moveable) with (frame)
(1235) ((chip die dice ic (integrated adj circuit)) same (bendable flexible moves
(430) (((chip die dice ic (integrated adj circuit)) same ((bendable flexible moves
(432) (((chip die dice ic (integrated adj circuit)) same ((bendable flexible move
(96375) ((bendable flexible moveable) with (frame container supporter))
(1033) ((bendable flexible moveable) with (frame container supporter)) and ((chip
(1235) (((bendable flexible moveable) with (frame container supporter)) and ((chip
(432) (((bendable flexible moveable) with (frame container supporter)) and ((chip
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DBs USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

Default operator: OR

Plurals

Highlight all hit terms initially

7 and [illegible]

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval C	Inventor	S	C	P
1			US 20030048200 A1	20030425	20	Integrated circuit memory devices having non-volatile	365/[illegible]			[illegible]	☑		
2			US 20020028[illegible] A1	20020307	15	METHODS OF FORMING RECESSED HEMISPHERICAL GRAIN SILICON	438/[illegible]			[illegible]	☑		
3			US 20020028541 A1	20020307	151	Dense arrays and charge storage devices, and methods	438/149			Lee, Thomas H. et al	☑		
4			US 20020027227 A1	20020307	25	SEMICONDUCTOR MEMORY DEVICE HAVING A TRENCH AND A GATE	257/[illegible]			KANG, SEEN-SUP	☑		
5			US 20020025479 A1	20020228	98	Process for fabricating semiconductor integrated	430/5	355/53; 438/31[illegible]		Okamoto, Yoshihiko et al	☑		
6			US 20020017701 A1	20020214	54	Electrically programmable memory element with raised	257/[illegible]			Klersy, Patrick et al	☑		
7			US 20020017629 A1	20020214	121	Semiconductor integrated circuit device, process for	257/296	[illegible]		[illegible]	☑		
8			US 2002001[illegible]6734 A1	20020117	24	Manufacturing method of semiconductor integrated	438/[illegible]	430/5; [illegible]		[illegible]	☑		
9			US 2002001[illegible]6555 A1	20020117	10[illegible]	Manufacturing method of photomask and photomask	430/5	430/311; 430/317;		Hasegawa, Norio et al	☑		
10			US 20020005543 A1	20020117	93	Manufacturing method of semiconductor integrated	257/306	438/241		Hayashi, Katsuya et al	☑		
11			US 20010055559 A1	20011220	20	Method of fabricating display device	433/23	433/27; 438/23		Nagai, Fitsuki et al	☑		

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Ready

1/1 PLUSPAT - (C) QUESTEL-ORBIT
PN - US5710461 A 19980120 [US5710461]
TI - (A) SRAM cell fabrication with interlevel dielectric planarization
PA - (A) SGS THOMSON MICROELECTRONICS (US)
IN - (A) NGUYEN LOI (US); SUNDARESAN RAVISHANKAR (US)
AP - US78142997 19970110 [1997US-0781429]
PR - US16933893 19931217 [1993US-0169338]
- US32873695 19951025 [1995US-0328736]
- US78142997 19970110 [1997US-0781429]
IC - (A) H01L-023/48 H01L-023/522 H01L-029/34 H01L-029/54
EC - H01L-021/3105B
- H01L-021/8244
PCL - ORIGINAL (O) : 257754000; CROSS-REFERENCE (X) : 257350000 257380000 257381000 257385000 257640000 257740000 257752000 257758000 257903000 257904000
DT - Basic
CT - US4676867; US4797717; US4920071; US4975875; US4990998; US5001539; US5077238; US5083190; US5110763; US5132774; US5151376; US5159416; US5169491; US5177238; US5188987; US5204288; US5219792; US5290399; US5319247; US5373170; US5381046; US5534731; US5552628; JP0099243; JP0135044; JP2251722; WO8700828
- IEEE Electron Device Letters, vol. 12, No. 3, Mar. 1991, Hot-Carrier Aging of the MOS Transistor in the Presence of Spin-On Glass as the interlevel Dielectric, by N. Lifshitz and G. Smolinsky, pp. 140-142.

Journal Electrochem. Soc., vol. 139, No. 2, Feb. 1992, Three "Lot Dt" Options for Planarizing the Pre-Metal Dielectric on an Advanced Double Poly BiCMOS Process, by W. Dauksher, M Miller, and C. Tracy, pp. 532-536.

Journal Electrochem. Soc., vol. 139, No. 2, Feb. 1992, Polysilicon Planarization Using Spin-On Glass, by Shrinath Ramaswami and Andrew Nagy, pp. 591-599.

Journal Electronicem. Soc., vol. 140, No. 4, Apr. 1993, The Effect of Plasma Cure Temperature on Spin-On Glass, by Hideo Namatsu and Kazushige Minegishi, pp. 1121-1125.
STG - (A) United States patent
AB - A 4-T SRAM cell in which two layers of permanent SOG (with an intermediate oxide layer) are used to provide planarization between the first and topmost poly layers.

1/1 LGST - (C) LEGSTAT
PN - US 5710461 [US5710461]
AP - US 781429/97 19970110 [1997US-0781429]
DT - US-P
ACT - 19970110 US/AE-A
APPLICATION DATA (PATENT)
{US 781429/97 19970110 [1997US-0781429]}
- 19980120 US/A
PATENT
- 20000307 US/RF
REISSUE APPLICATION FILED
20000120
UP - 2000-10

1/1 CRXX - (C) CLAIMS/RRX
AN - 2933021
PN - 5,710,461 A 19980120 [US5710461]
PT - E (Electrical)
PA - SGS-Thomson Microelectronics Inc
ACT - 20000120 REISSUE REQUESTED
Issue Date of O.G.: 20000307
Reissue Request Number: 09/488686
Examination Group responsible for Reissue process: 2811

UP - 2000-10
UACT- 2000-03-07

1/1 PAST - (C) PAST
AN - 200010-001243
PN - 5710461 A [US5710461]
DT - A (UTILITY)
OG - 2000-03-07
CO - REA
ACT - REISSUE APPLICATION FILED
SH - REISSUE APPLICATION FILED

1/39/4
DIALOG(R)File 345:Inpadoc/Fam.& Legal Stat

12262040
Basic Patent (No,Kind,Date): US 5395785 A 19950307 <No. of Patents: 002>
Patent Family:

Patent No	Kind	Date	Applic No	Kind	Date	
US 5395785	A	19950307	US 169338	A	19931217	(BASIC)
US 5710461	A	19980120	US 781429	A	19970110	

Priority Data (No,Kind,Date):
US 169338 A 19931217
US 781429 A 19970110
US 328736 B1 19951025
US 169338 A3 19931217

PATENT FAMILY:
UNITED STATES OF AMERICA (US)
Patent (No,Kind,Date): US 5395785 A 19950307
SRAM CELL FABRICATION WITH INTERLEVEL DIELECTRIC PLANARIZATION (English)
Patent Assignee: SGS THOMSON MICROELECTRONICS (US)
Author (Inventor): NGUYEN LOI (US); SUNDARESAN RAVISHANKAR (US)
Priority (No,Kind,Date): US 169338 A 19931217
Applic (No,Kind,Date): US 169338 A 19931217
National Class: * 437052000; 437047000; 437060000; 437235000; 437919000
IPC: * H01L-021/70
CA Abstract No: * 122(24)304566E; 122(24)304566E
Derwent WPI Acc No: * C 95-114834; C 98-238649; C 95-114834
Language of Document: English
Patent (No,Kind,Date): US 5710461 A 19980120
SRAM CELL FABRICATION WITH INTERLEVEL DIELECTRIC PLANARIZATION (English)
Patent Assignee: SGS THOMSON MICROELECTRONICS (US)
Author (Inventor): NGUYEN LOI (US); SUNDARESAN RAVISHANKAR (US)
Priority (No,Kind,Date): US 781429 A 19970110; US 328736 B1 19951025; US 169338 A3 19931217
Applic (No,Kind,Date): US 781429 A 19970110
Addnl Info: 5395785 Patented
National Class: * 257754000; 257760000; 257640000; 257904000; 257752000; 257903000; 257350000; 257380000; 257381000; 257385000; 257758000
IPC: * H01L-029/34; H01L-023/48; H01L-023/522; H01L-029/54
CA Abstract No: * 122(24)304566E
Derwent WPI Acc No: * C 95-114834; C 98-238649; C 98-238649
Language of Document: English

UNITED STATES OF AMERICA (US)
Legal Status (No,Type,Date,Code,Text):

US 5395785	P	19931217	US AE	APPLICATION DATA (PATENT) (APPL. DATA (PATENT)) US 169338 A 19931217
US 5395785	P	19931217	US AS02	ASSIGNMENT OF ASSIGNOR'S INTEREST SGS-THOMSON MICROELECTRONICS, INC. 1310 ELECTRONICS DRIVE CARROLLTON, TX 75006- ;

NGUYEN, LOI N. : 19931217; SUNDARESAN, RAVISHANKAR : 19931217

US 5395785	P	19950307	US	A	PATENT
US 5710461	P	19931217	US	AA	PRIORITY
		US 169338	A3	19931217	
US 5710461	P	19951025	US	AA	PRIORITY
		US 328736	B1	19951025	
US 5710461	P	19970110	US	AE	APPLICATION DATA (PATENT)
		(APPL. DATA (PATENT))			
		US 781429	A	19970110	
US 5710461	P	19980120	US	A	PATENT
US 5710461	P	20000307	US	RF	REISSUE APPLICATION FILED
		(REISSUE APPL. FILED)			
		20000120			